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(54) **IMAGE SENSOR, AN INSPECTION SYSTEM
AND A METHOD OF INSPECTING AN
ARTICLE**

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patent is extended or adjusted under 35
U.S.C. 154(b) by 0 days.

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17, 2014.

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G01N 21/95 (2006.01)
(Continued)

(52) **U.S. Cl.**
CPC **G01N 21/9501** (2013.01); **G01N 21/8806**
(2013.01); **H01L 27/1461** (2013.01); **H01L**
27/1464 (2013.01); **H01L 27/14609** (2013.01);
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CPC H01L 27/1464
See application file for complete search history.

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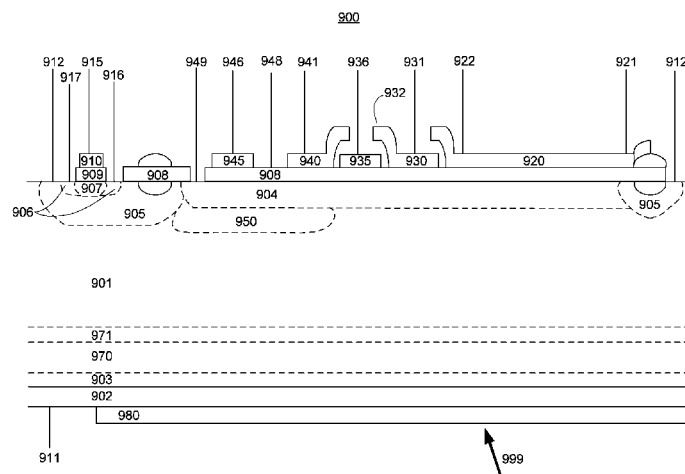
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(57) **ABSTRACT**

A high sensitivity image sensor comprises an epitaxial layer
of silicon that is intrinsic or lightly p doped (such as a doping
level less than about 10^{13} cm^{-3}). CMOS or CCD circuits are
fabricated on the front-side of the epitaxial layer. Epitaxial p
and n type layers are grown on the backside of the epitaxial
layer. A pure boron layer is deposited on the n-type epitaxial
layer. Some boron is driven a few nm into the n-type epitaxial
layer from the backside during the boron deposition process.
An anti-reflection coating may be applied to the pure boron
layer. During operation of the sensor a negative bias voltage
of several tens to a few hundred volts is applied to the boron
layer to accelerate photo-electrons away from the backside
surface and create additional electrons by an avalanche effect.
Grounded p-wells protect active circuits as needed from the
reversed biased epitaxial layer.

19 Claims, 10 Drawing Sheets



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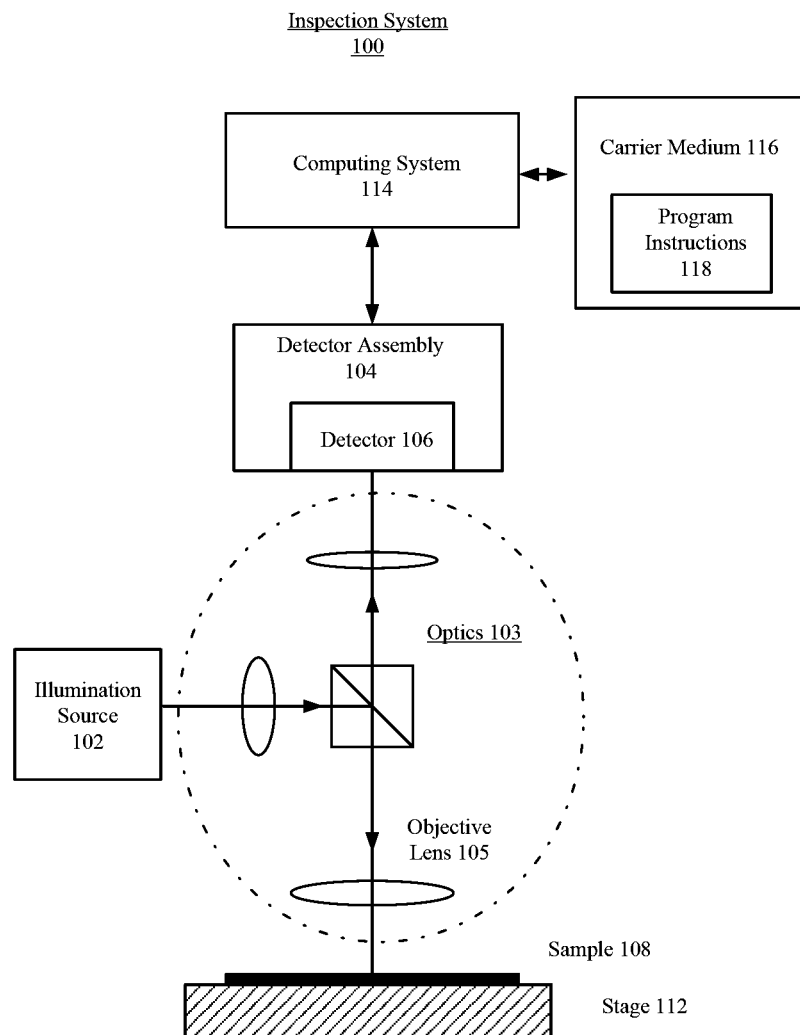


Figure 1

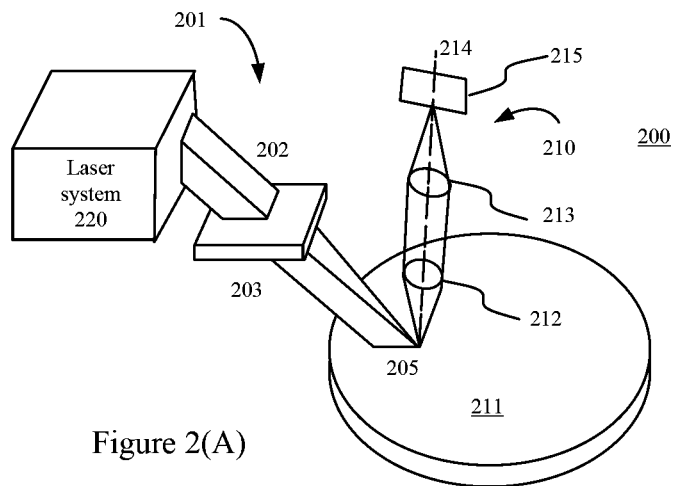


Figure 2(A)

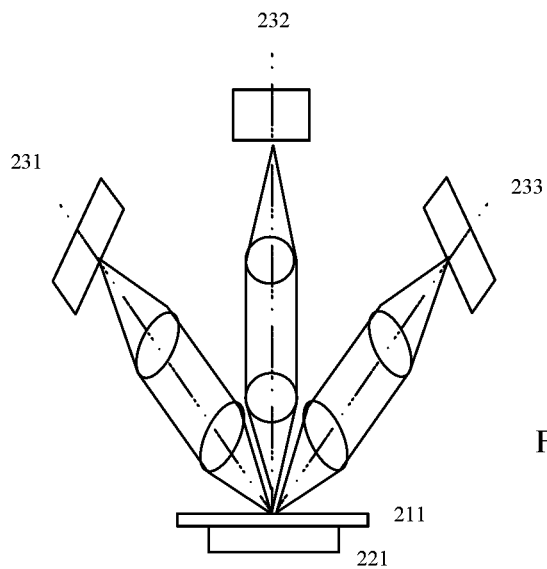


Figure 2(B)

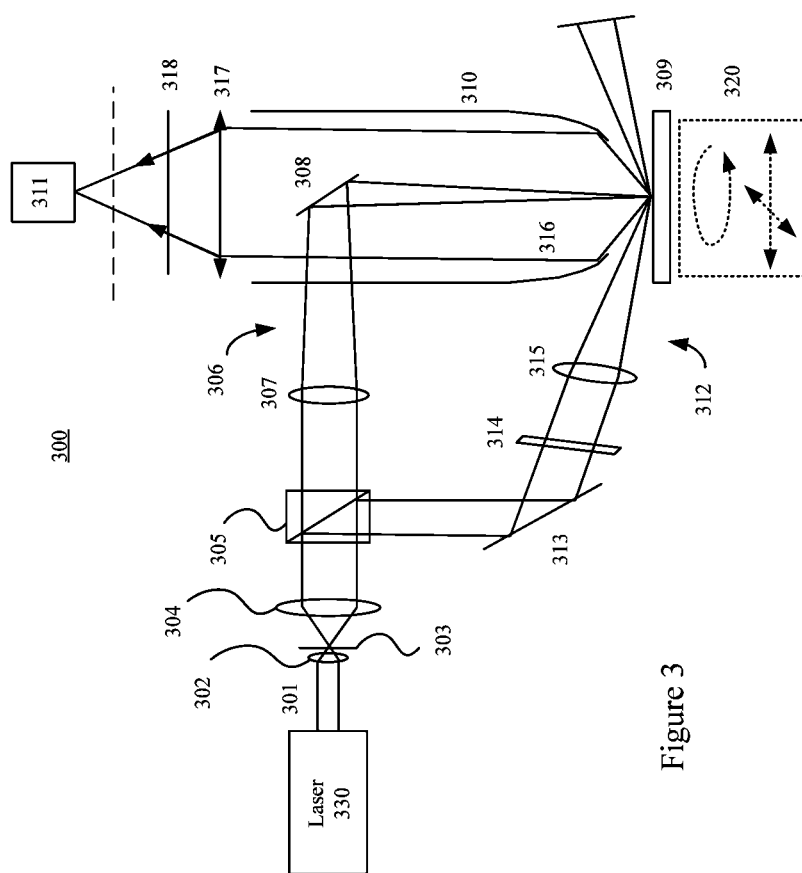


Figure 3

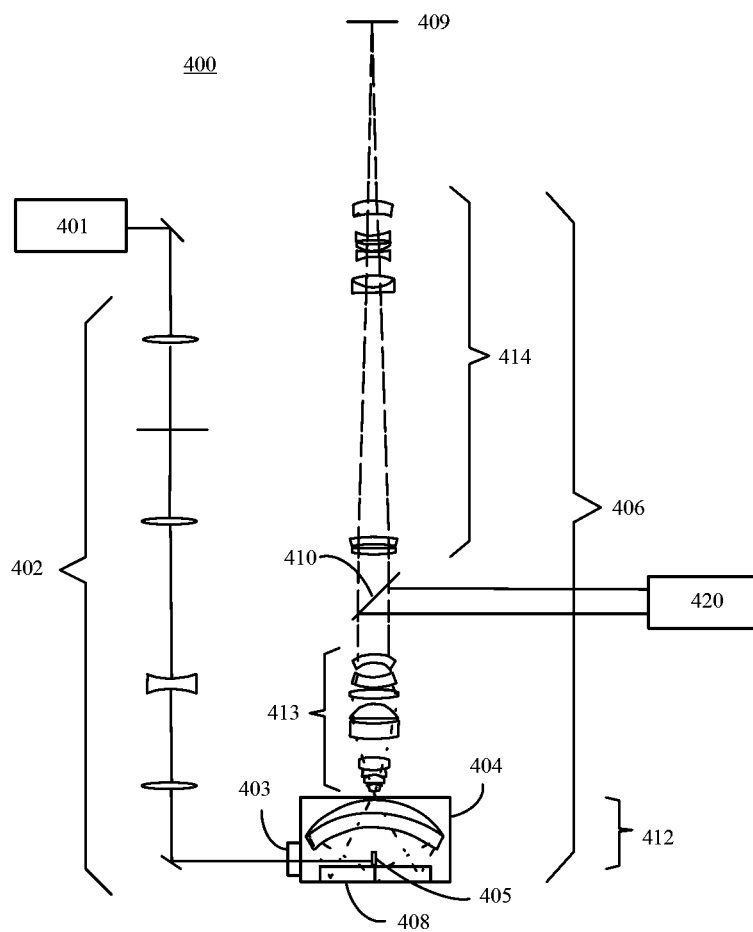


Figure 4

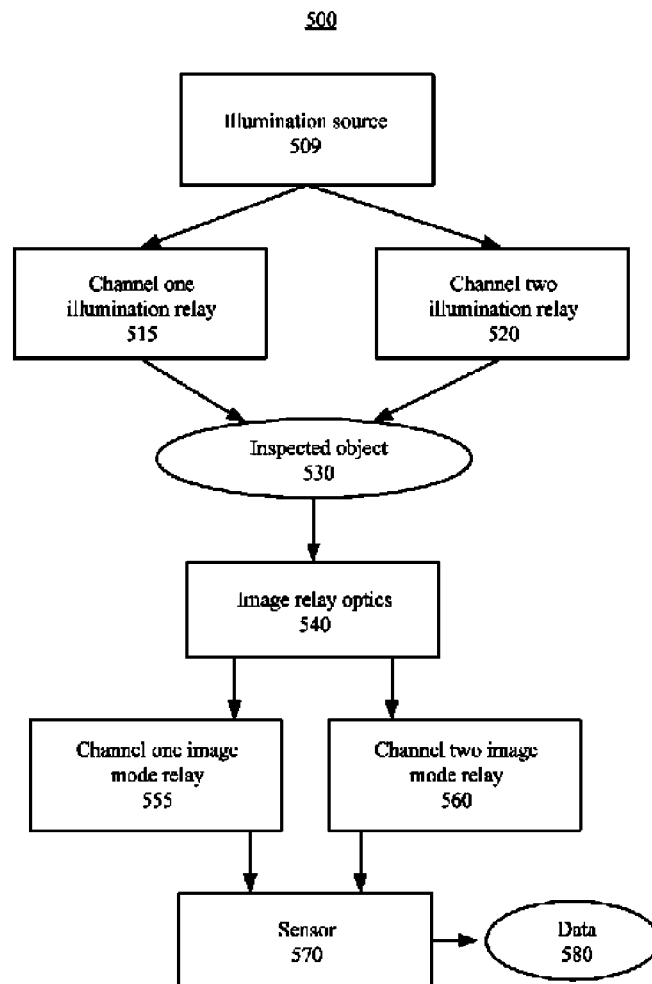


Figure 5

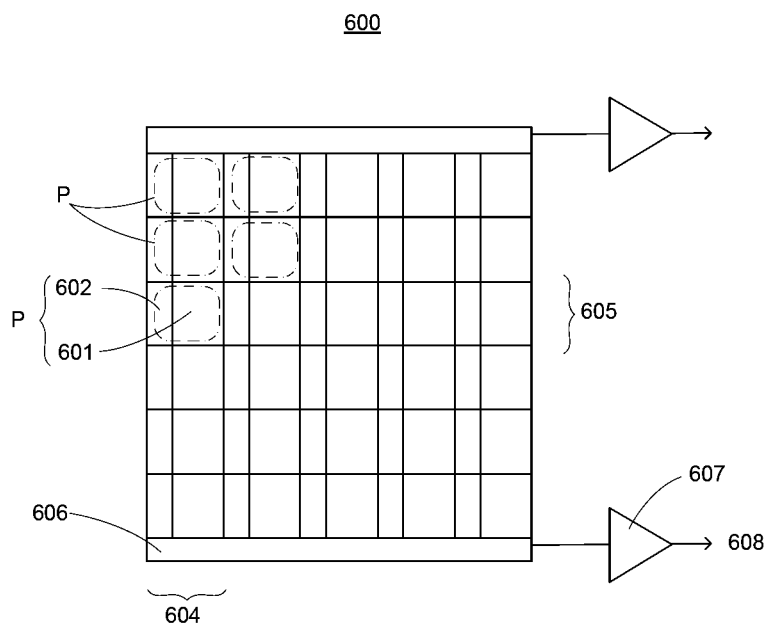


FIG. 6

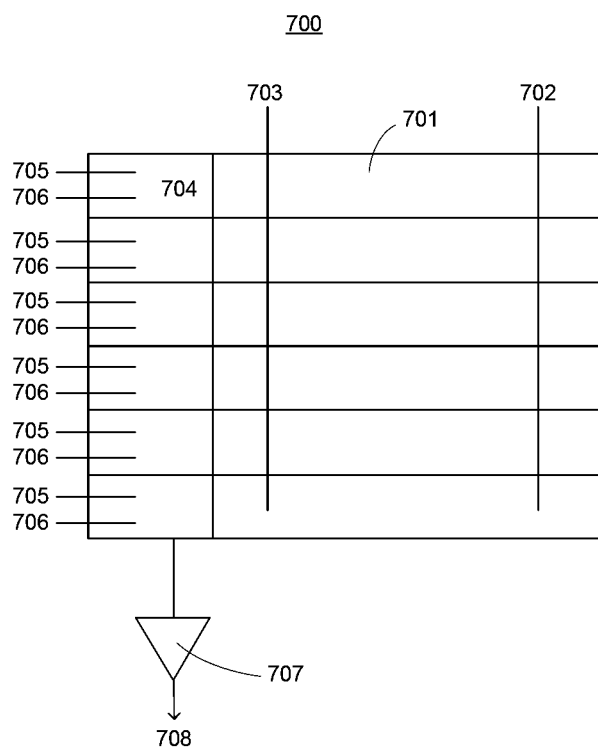


FIG. 7

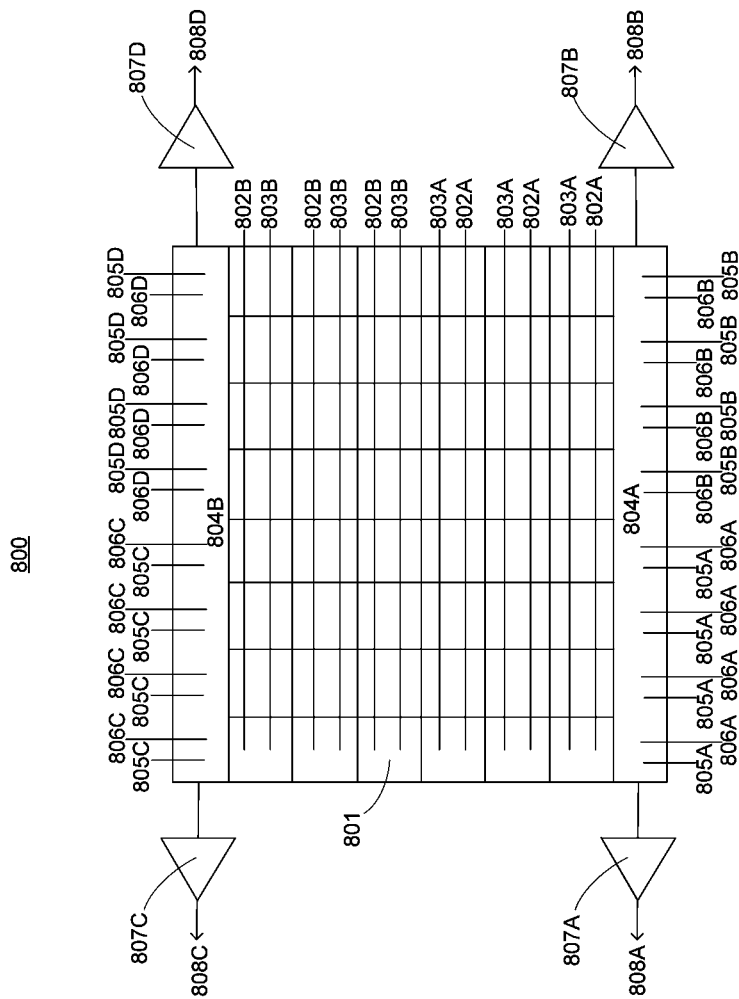
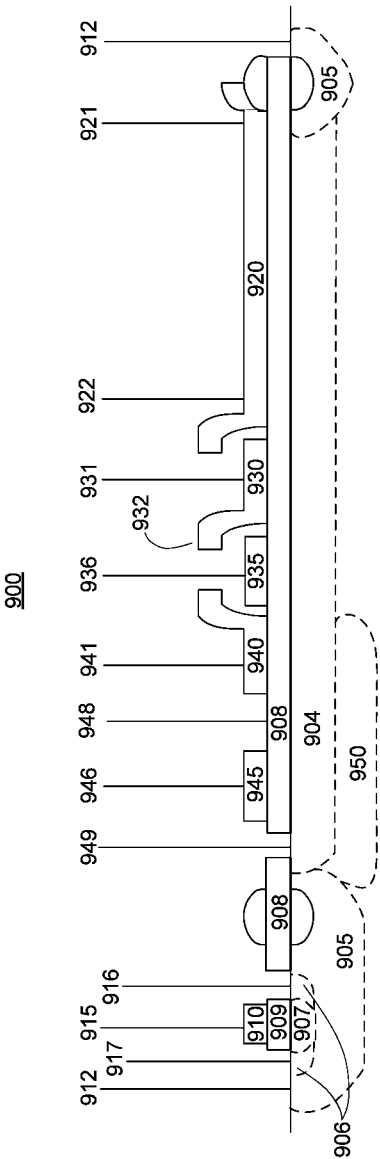


FIG. 8



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FIG. 9

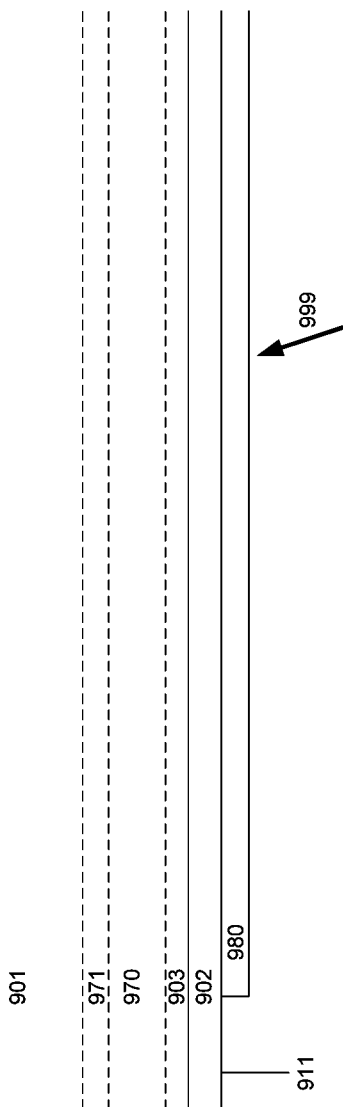
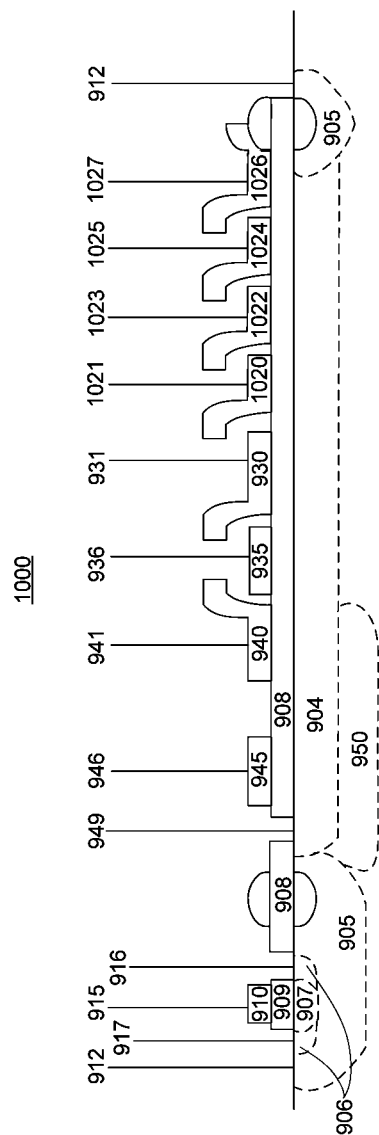


IMAGE SENSOR, AN INSPECTION SYSTEM AND A METHOD OF INSPECTING AN ARTICLE

RELATED APPLICATIONS

The present application claims priority to U.S. Provisional Patent Application 61/954,328, entitled "AN IMAGE SENSOR, AN INSPECTION SYSTEM AND A METHOD OF INSPECTING AN ARTICLE", filed on Mar. 17, 2014, and incorporated by reference herein.

The present application is related to U.S. patent application Ser. No. 14/273,424 entitled "Low-Noise Sensor And An Inspection System Using A Low-Noise Sensor" and filed by Brown et al. on May 8, 2014, to U.S. patent application Ser. No. 11/805,907 entitled "Inspection System Using Back Side Illuminated Linear Sensor" and filed by Armstrong et al. on May 25, 2007, to U.S. patent application Ser. No. 13/364,308 entitled "High-density digitizer" and filed by Brown et al. on Feb. 1, 2012, to U.S. patent application Ser. No. 14/096,911 entitled "Method and apparatus for high-speed acquisition of moving images using pulsed illumination" and filed by Brown et al. on Dec. 4, 2013, to U.S. patent application Ser. No. 13/622,155 entitled "Interposer Based Imaging Sensor for High-Speed Image Acquisition and Inspection Systems" and filed by Brown et al. on Sep. 18, 2012, and to U.S. patent application Ser. No. 13/792,166 entitled "Back-Illuminated Sensor With Boron Layer" and filed by Chern et al. on Mar. 10, 2013. It is also related to U.S. Pat. No. 7,609,309 entitled "Continuous Clocking of TDI Sensors" to Brown et al., U.S. Pat. No. 7,952,633 entitled "Apparatus for Continuous Clocking of TDI Sensors" to Brown et al., and U.S. Pat. No. 8,624,971 "TDI Sensor Modules with Localized Driving and Signal Processing Circuitry for High Speed Inspection" to Brown et al. All of these patents and applications are incorporated by reference herein.

BACKGROUND OF THE DISCLOSURE

1. Field of the Disclosure

The present application relates to images sensors suitable for detecting images at vacuum UV (VUV), deep UV (DUV), visible and near infra-red (NIR) wavelengths, and to inspection systems incorporating such sensors. In particular it relates to sensors and methods for fabricating sensors with low noise and high sensitivity. The sensors are particularly suitable for use in inspection systems including those used to inspect photomasks, reticles, and semiconductor wafers.

2. Related Art

The integrated circuit industry requires inspection tools with increasingly higher sensitivity to detect ever smaller defects and particles including those with dimensions close to 10 nm or smaller. Furthermore these inspection tools must operate at high speed in order to inspect 100%, or a large fraction, of the area of a photomask, reticle or wafer, usually in less than one hour. Some applications require many (such as about 50 or 100) wafers to be inspected in one hour. Generally short wavelengths such as UV, deep UV (DUV) and vacuum UV (VUV) wavelengths have higher sensitivity for detecting small defects and particles compared with longer wavelengths. Inspection of photomasks or reticles is best done using the same wavelength as used for lithography, which is currently a wavelength of substantially 193.4 nm for the most critical lithography steps and substantially 248 nm for less critical steps. High-speed inspection requires sensors with high sensitivity and low noise in order to detect the small amount of light scattered from small particles or defects or

allow detection of small changes in reflectivity due to defects in the pattern. An image sensor that can detect a change in light level of one, or a few, photons is highly desirable.

Silicon CMOS and CCD image sensors are known in the art. CCD image sensors are particularly suitable for high-speed inspection systems for semiconductor wafers, photomasks and reticles because the electronic noise of such sensors is quite low and follows closely a Poisson statistical distribution (apart from very infrequent events caused by absorption of charged particles from cosmic rays or radioactive decay, which are rare and can generally be filtered out by image processing software). Silicon CCD image sensors can have noise levels equivalent to about 2 electrons RMS if the sensor is cooled to about 100° K and is read out at a relatively low speed (such as a rate of a few hundred thousand pixels per second or less) and appropriate driving and reading electronics are used. Such sensors, when operated at similar speeds, but at a temperature closer to room temperature (such as about -10° C.) may have noise levels equivalent to about 5-10 electrons RMS. However high-speed inspection systems require data rates of multiple billions of pixels per second, which are generally achieved by reading many tens or a few hundred pixels (taps) simultaneously at rates of several to a few tens of millions of pixels per second. Such high data rates and so many output channels operating at the same time generate many Watts of heat making cooling below room temperature impractical. The high speed operation itself also generates more electrical noise and, when combined with the high operating temperature, can lead to noise levels equivalent to about 20 to 40 electrons RMS.

CMOS sensors typically have higher noise levels than CCD sensors because CMOS transistors have their channels on the surface of the silicon resulting in noise from the silicon to silicon dioxide interface (due to defects and traps at that interface). Furthermore this noise from the surface defects and traps does not closely follow Poisson statistics. Even if the RMS noise is low, high noise spikes are much more frequent than would be expected from Poisson statistics. This is a serious problem for inspection systems, as these high noise spikes can result in a false detection of a defect. Systems with a CMOS detector may have high rates of reporting false defect rates when operated in their highest sensitivity modes. A reinspection would be needed to separate false from true defects, slowing down the inspection.

For UV wavelengths, when a photon is absorbed in silicon, usually only a single electron-hole pair is created, but occasionally two pairs may be created, resulting in average yield per absorbed photon slightly greater than 1. At DUV and VUV wavelengths, the probability of a second electron-hole pair being produced increases so the average electron yield increases. For example, when photons of a vacuum wavelength of 193 nm are absorbed in silicon, the average yield is about 1.7 electron-hole pairs per absorbed photon. For wavelengths currently used in semiconductor inspection systems and wavelengths likely to be used within the next several years, the electron-hole pair yield will not exceed 2. Hence silicon CCD and CMOS sensors are not able to reliably detect one, or a few, photons when sensing visible, UV, DUV or VUV wavelengths.

Avalanche photodiodes are known in the art. An avalanche photodiode uses a relatively large reverse bias voltage (tens to a few hundred volts) over a distance of about one hundred or a few hundred microns of silicon in order to generate multiple carriers (electrons or holes) from a single carrier created by photon absorption. When a photon is absorbed, an electron-hole pair is created, usually close to the surface when sensing UV radiation because of the strong absorption of silicon at

UV wavelengths. The bias voltage accelerates the carriers. When a carrier has accelerated to a high enough speed to have about 3.7 eV of energy, it can create an additional electron-hole pair by collision. This process can be repeated a few times creating more carriers and, hence, a large signal.

Most common avalanche diodes absorb the incident light in n-type silicon and apply a bias voltage to accelerate holes away from the surface. This is because surface defects on the silicon tend to have positive charges and attract electrons. Furthermore, to make an avalanche detector that uses electrons rather than holes requires doping the light absorbing silicon to p-type silicon. Boron is the only practically useful p-type dopant for silicon. Boron diffuses easily into silicon dioxide create positive charges in the oxide. This further increases the electron recombination rate at the surface and makes conventional electron-based avalanche photodiodes less efficient for UV, DUV and VUV wavelengths. The avalanche gain and mobility are both lower for holes than electrons in silicon. So avalanche diodes using holes need a longer length in silicon and/or a higher operating voltage in order to achieve a given gain factor.

Therefore, a need arises for a sensor overcoming some, or all, of the above disadvantages. In particular a need arises for an image sensor that can detect very low levels of UV, DUV and/or VUV light while operating at very high data rates, such as billions of pixels per second.

SUMMARY OF THE DISCLOSURE

An exemplary inspection system is described. This inspection system includes an illumination source, optics, and a detector. The illumination source includes a UV, DUV or VUV laser that generates light at one, or a few, discrete wavelengths, or the illumination source includes laser-sustained plasma light source that emits broadband light including light at UV, DUV and/or VUV wavelengths. The optics are configured to direct and focus radiation from the illumination source onto a sample. The sample is supported by a stage, which moves relative to the optics during the inspection. The detector is configured to receive reflected or scattered light from the sample, wherein the optics are further configured to collect, direct, and focus the reflected or scattered light onto the detector. The detector includes one or more backside-illuminated avalanche image or line sensors as described below. In one embodiment, at least one image sensor is a backside-illuminated avalanche time delay integration (TDI) sensor.

The exemplary inspection system may include one or more illumination paths that illuminate the sample from different angles of incidence and/or different azimuth angles and/or with different wavelengths and/or polarization states. The exemplary inspection system may include one or more collection paths that collect light reflected or scattered by the sample in different directions and/or are sensitive to different wavelengths and/or to different polarization states. The exemplary inspection system may include a backside-illuminated avalanche TDI sensor with readout circuits on two sides that are used to read out two different signals simultaneously.

An exemplary method of inspecting a sample is described. The exemplary method includes directing and focusing radiation from an illumination source onto the sample. The sample is supported by a stage, which moves relative to the optics during the inspection. The method further includes using optics to collect, direct, and focus light reflected or scattered by the sample onto a detector. The detector includes one or

more backside-illuminated avalanche image or line sensors. At least one image sensor may be a backside-illuminated avalanche TDI sensor.

Exemplary backside-illuminated avalanche image and line sensors are described. The exemplary image and line sensors may be fabricated with CMOS or CCD technology. The exemplary image and line sensors use electrons to detect near-IR, visible, UV, DUV and/or VUV light with high quantum efficiency. The exemplary image and line sensors incorporate a pure boron layer on their backside (illuminated) surface. The pure boron layer prevents growth of a native oxide on that surface. Furthermore some of the boron diffuses a short distance into the silicon to create a highly doped p-type semiconductor layer just beneath the surface. This p-type layer, in combination with the applied backside negative bias voltage drives electrons away from the surface and minimizes recombination of photo-electrons at or near the surface.

An exemplary method for fabricating backside-illuminated avalanche image and line sensors is described. This method includes fabricating front-side CMOS or CCD circuits and pixels in an intrinsic or lightly p-type doped (such as about 10^{11} to 2×10^{13} dopant atoms per cubic centimeter (cm^3)) epitaxial layer of silicon on a silicon wafer. After the front-side circuits are at least partially fabricated, the wafer is polished or etched to expose, at least, the light sensitive (backside) area. This method further includes depositing a thin (such as 2 nm to 6 nm thick) pure boron layer on the backside surface of the epitaxial silicon layer. In some embodiments, during the boron deposition, the wafer is kept at an elevated temperature (such as 700°C . to 950°C .) for a few minutes, or a few tens of minutes, to drive in some of the boron as a dopant of the silicon.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 illustrates an exemplary inspection system incorporating a detector that comprises a backside-illuminated avalanche image or line sensor.

FIGS. 2A and 2B illustrate an exemplary inspection system using line illumination with one, or more, collection channels and one, or more, backside-illuminated avalanche line sensors.

FIG. 3 illustrates an exemplary inspection system with normal and oblique illumination and a backside-illuminated avalanche image or line sensor.

FIG. 4 illustrates an exemplary inspection system with bright-field and dark-field illumination channels and a backside-illuminated avalanche image sensor.

FIG. 5 illustrates an exemplary inspection system incorporating a split-readout backside illuminated avalanche image sensor.

FIG. 6 illustrates an exemplary layout of a two-dimensional (2D) CMOS image sensor incorporating backside-illuminated avalanche sensing.

FIG. 7 illustrates an exemplary layout of a line sensor incorporating backside-illuminated avalanche sensing.

FIG. 8 illustrates an exemplary layout of a 2D CCD image sensor incorporating backside-illuminated avalanche sensing.

FIG. 9 illustrates key aspects of the design and fabrication of back-side illuminated avalanche image and line sensors.

FIG. 10 illustrates key aspects of the design and fabrication of a back-side illuminated avalanche image sensor using CCD technology.

DETAILED DESCRIPTION OF THE DRAWINGS

The present invention relates to an improvement in sensors for semiconductor inspection systems. The following

description is presented to enable one of ordinary skill in the art to make and use the invention as provided in the context of a particular application and its requirements. As used herein, directional terms such as “top”, “bottom”, “over”, “under”, “upper”, “upward”, “lower”, “down”, “downward”, “front-side” and “backside” are intended to provide relative positions for purposes of description, and are not intended to designate an absolute frame of reference. As used herein, the terms image sensor and line sensor are interchangeable except where the description is of a sensor explicitly comprising a 2D array of pixels (generally called an image sensor) or where the description is of a sensor explicitly consisting of a 1D line of pixels (generally called a line sensor). Various modifications to the preferred embodiment will be apparent to those with skill in the art, and the general principles defined herein may be applied to other embodiments. Therefore, the present invention is not intended to be limited to the particular embodiments shown and described, but is to be accorded the widest scope consistent with the principles and novel features herein disclosed.

FIG. 1 illustrates an exemplary inspection system **100** configured to measure a sample **108** such as a wafer, reticle, or photomask. Sample **108** is placed on a stage **112** in order to facilitate movement to different regions of sample **108** underneath the optics. Stage **112** may comprise an X-Y stage or an R- θ stage. In some embodiments, stage **112** can adjust the height of sample **108** during inspection to maintain focus. In other embodiments, an objective lens **105** can be adjusted to maintain focus.

An illumination source **102** may comprise one or more lasers and/or a broad-band light source. Illumination source **102** may emit DUV and/or VUV radiation. Optics **103** including an objective lens **105** directs that radiation towards, and focuses it on, sample **108**. Optics **103** may also comprise mirrors, lenses, and/or beam splitters. Light reflected or scattered from sample **108** is collected, directed, and focused by optics **103** onto a detector **106**, which is within a detector assembly **104**.

Detector assembly **104** includes a detector **106**. Detector **106** comprises a backside-illuminated avalanche image or line sensor as described herein. Detector **106** may include a two-dimensional image sensor or a one-dimensional line sensor. In one embodiment, the output of detector **106** is provided to a computing system **114**, which analyzes the output. Computing system **114** is configured by program instructions **118**, which can be stored on a carrier medium **116**.

One embodiment of inspection system **100** illuminates a line on sample **108**, and collects scattered and/or reflected light in one or more dark-field and/or bright-field collection channels. In this embodiment, the detector **106** may include a backside-illuminated avalanche line sensor.

Another embodiment of inspection system **100** illuminates multiple spots on sample **108**, and collects scattered and/or reflected light in one or more dark-field and/or bright-field collection channels. In this embodiment, the detector **106** may include a two-dimensional backside-illuminated avalanche image sensor, or it may comprise multiple discrete backside illuminated avalanche sensors.

Additional details of various embodiments of inspection system **100** can be found in U.S. patent application Ser. No. 13/554,954, entitled “WAFER INSPECTION SYSTEM”, filed on Jul. 9, 2012 by Romanovsky et al., U.S. Published Patent Application 2009/0180176, by Armstrong et al., which published on Jul. 16, 2009, U.S. Published Patent Application 2007/0002465 by Chuang et al., which published on Jan. 4, 2007, U.S. Pat. No. 5,999,310, by Shafer et al., which issued on Dec. 7, 1999, and U.S. Pat. No. 7,525,649 by Leong et al.,

which issued on Apr. 28, 2009. All of these patents and patent applications are incorporated by reference herein.

FIGS. 2(A) and 2(B) illustrate aspects of dark-field inspection systems that incorporate the sensors and/or methods described herein in accordance with other exemplary embodiments of the present invention. In FIG. 2(A), illumination optics **201** comprises a DUV or VUV laser system **220** generating light **202** that is focused by mirror or lens **203** into a line **205** on the surface of the wafer or photomask (sample) **211** being inspected. Collection optics **210** directs light scattered from line **205** to sensor **215** using lenses and/or mirrors such as **212** and **213**. The optical axis **214** of the collection optics is not in the illumination plane of line **205**. In some embodiments, axis **214** is approximately perpendicular to the line **205**. Sensor **215** comprises a back-illuminated avalanche array sensor, such as a back-illuminated avalanche line sensor as described herein.

FIG. 2(B) illustrates one embodiment of multiple dark-field collection systems (**231**, **232** and **233**, respectively) each substantially similar to the collection optics **210** of FIG. 2(A). Collection systems **231**, **232** and **233** are used in combination with illumination optics substantially similar to illumination optics **201** in FIG. 2(A). One of more of the dark-field collection systems include a back-illuminated avalanche image or line sensor. Sample **211** is supported on stage **221**, which moves the areas to be inspected underneath the optics. Stage **221** may comprise an X-Y stage or an R- θ stage, which preferably moves substantially continuously during the inspection in order to inspect large areas of the sample with minimal dead time.

More details of inspection systems in accordance with the embodiments illustrated in FIGS. 2(A) and 2(B) can be found in U.S. Pat. No. 7,525,649, U.S. Pat. No. 6,608,676, which is incorporated by reference herein, also describes line illumination systems suitable for inspection of unpatterned or patterned wafers.

FIG. 3 illustrates an inspection system **300** configured to detect particles or defects on a sample using both normal and oblique illumination beams. In this configuration, a DUV or VUV laser system **330** provides a laser beam **301**. A lens **302** focuses the beam **301** through a spatial filter **303**. Lens **304** collimates the beam and conveys it to a polarizing beam splitter **305**. Beam splitter **305** passes a first polarized component to the normal illumination channel and a second polarized component to the oblique illumination channel, where the first and second components are orthogonal. In the normal illumination channel **306**, the first polarized component is focused by optics **307** and reflected by mirror **308** towards a surface of a sample **309**. The radiation scattered by sample **309** (such as a wafer or photomask) is collected and focused by a paraboloidal mirror **310** to backside illuminated avalanche sensor **311**.

In the oblique illumination channel **312**, the second polarized component is reflected by beam splitter **305** to a mirror **313** which reflects such beam through a half-wave plate **314** and focused by optics **315** to sample **309**. Radiation originating from the oblique illumination beam in the oblique channel **312** and scattered by sample **309** is collected by paraboloidal mirror **310** and focused to backside-illuminated avalanche sensor **311**. The sensor and the illuminated area (from the normal and oblique illumination channels on surface **309**) are preferably at the foci of the paraboloidal mirror **310**.

The paraboloidal mirror **310** collimates the scattered radiation from sample **309** into a collimated beam **316**. Collimated beam **316** is then focused by an objective **317** and through an analyzer **318** to the sensor **311**. Note that curved mirrored surfaces having shapes other than paraboloidal shapes may

also be used. An instrument **320** can provide relative motion between the beams and sample **309** so that spots are scanned across the surface of sample **309**. U.S. Pat. No. 6,201,601, which issued on Mar. 13, 2001 and is incorporated by reference herein, describes inspection system **300** in further detail.

FIG. 4 illustrates an exemplary catadioptric imaging system **400** configured as an inspection system with bright-field and dark-field inspection modes. System **400** may incorporate two illuminations sources: a laser **401**, and a broad-band light illumination module **420**.

In a dark-field mode, adaptation optics **402** control the laser illumination beam size and profile on the surface being inspected. Mechanical housing **404** includes an aperture and window **403**, and a prism **405** to redirect the laser along the optical axis at normal incidence to the surface of a sample **408**. Prism **405** also directs the specular reflection from surface features of sample **408** out of objective **406**. Objective **406** collects light scattered by sample **408** and focuses it on sensor **409**. Lenses for objective **406** can be provided in the general form of a catadioptric objective **412**, a focusing lens group **413**, and a tube lens section **414**, which may, optionally, include a zoom capability.

In a bright-field mode, broad-band illumination module **420** directs broad-band light to beam splitter **410**, which reflects that light towards focusing lens group **413** and catadioptric objective **412**. Catadioptric objective **412** illuminates the sample **408** with the broadband light. Light that is reflected or scattered from the sample is collected by objective **406** and focused on sensor **409**. Broad-band illumination module **420** comprises, for example, a laser-sustained plasma light source or an arc lamp. Broad-band illumination module **420** may also include an auto-focus system to provide a signal to control the height of sample **408** relative to catadioptric objective **412**.

Sensor **409** includes a backside-illuminated avalanche image sensor as described herein. In one embodiment, sensor **409** comprises a backside illuminated avalanche image sensor, which is used for dark-field imaging, and a backside illuminated image sensor, which is used for bright-field imaging. Both image sensors may operate in a TDI mode.

Published Patent Application 2007/0002465, which published on Jan. 4, 2007 and is incorporated by reference herein, describes system **400** in further detail.

FIG. 5 shows a reticle, photomask or wafer inspection system **500** that simultaneously detects two channels of image or signal on one backside illuminated avalanche image sensor **570**. Backside illuminated avalanche image sensor **570** comprises a split-readout image sensor. Illumination source **509** incorporates a DUV laser. The operating wavelength of the DUV laser may be shorter than about 200 nm, such as a wavelength of approximately 193 nm. The two channels may comprise reflected and transmitted intensity when an inspected object **530** is transparent (for example a reticle or photomask), or may comprise two different illumination modes, such as angles of incidence, polarization states, wavelength ranges or some combination thereof. The light is directed to inspected object **530** using channel one illumination relay **515** and channel two illumination relay **520**.

The inspected object **530** may be a reticle, a photomask, a semiconductor wafer or other article to be inspected. Image relay optics **540** can direct the light that is reflected and/or transmitted by inspected object **530** to a channel one image mode relay **555** and to a channel two image mode relay **560**. Channel one image mode relay **555** is tuned to detect the reflection or transmission corresponding to channel one illumination relay **515**, whereas channel two image mode relay sensor **560** is tuned to detect the reflection or transmission

corresponding to channel two illumination relay **520**. Channel one image mode relay **555** and channel two image mode relay sensor **560** in turn direct their outputs to backside illuminated avalanche sensor **570**. The data corresponding to the detected signals or images for the two channels is shown as data **590** and is transmitted to a computer (not shown) for processing.

Other details of reticle and photomask inspection systems and methods that may be configured to measure transmitted and reflected light from a reticle or photomask are described in U.S. Pat. No. 7,352,457, which issued to Kvamme et al. on Apr. 1, 2008, and in U.S. Pat. No. 5,563,702, which issued to Emery et al. on Oct. 8, 1996, both of which are incorporated by reference herein.

Additional details regarding exemplary embodiments of image sensor **570** are provided in U.S. patent application Ser. No. 14/096,911, entitled "METHOD AND APPARATUS FOR HIGH SPEED ACQUISITION OF MOVING IMAGES USING PULSED ILLUMINATION", filed by Brown et al. on Dec. 4, 2013, and in U.S. Pat. No. 7,528,943 entitled "METHOD AND APPARATUS FOR SIMULTANEOUS HIGH-SPEED ACQUISITION OF MULTIPLE IMAGES" by Brown et al., which issued on May 5, 2009. These patents and patent applications are incorporated by reference herein.

FIG. 6 shows an exemplary layout of a 2D backside-illuminated avalanche image sensor **600** based on CMOS imaging technology. The image sensor comprises a 2D array of pixels **P** which, in turn, comprise a light signal collecting area **601** and associated pixel circuits **602**. The pixels are laid out in columns such as **604** and rows such as **605**. Key features of a pixel are illustrated in FIG. 9, which is described below. A row select signal (not shown) directs all the pixels of one row to output their signals. Column selector **606** can select one column and direct its signal to an output such as **608**, via a buffer, amplifier or analog-to-digital converter **607**. Image sensor **600** may output its signal in analog or digital format. Typically image sensor **600** has multiple outputs in order to be able to output image data at a total data rate of billions of pixels per second.

FIG. 7 shows an exemplary layout of a backside-illuminated avalanche line sensor **700**. Multiple pixels such as **701** are laid out in one line. Two or more control voltages **702** and **703** are connected to the pixels to control where the electrons accumulate within the pixel as explained below in the description of FIG. 9. In one embodiment each pixel connects to a readout register **704**. The readout registers are arranged in a line. Horizontal clocks **705** and **706** control the transfer of electrons from one horizontal register to the next so as to allow the signal to be sent to **707** which comprises a charge-to-voltage converter, a buffer and, optionally, an amplifier to drive output **708**. In preferred embodiments (not shown), the readout registers are divided into multiple segments so that multiple outputs are used with between about 4 and about 128 pixels connect to one output. In another embodiment there is one output for every two pixels and no readout register transfer is needed. In another embodiment, charge-to-voltage conversion, buffering and, optionally, amplification, is done at each pixel and the output registers are replaced by a series of switches to allow each pixel to be connected to the output in turn. In such an embodiment multiple outputs are preferred with between 2 and 128 pixels per output.

FIG. 8 shows an exemplary layout of a 2D backside-illuminated avalanche image sensor **800** based on CCD imaging technology. Multiple pixels such as **801** are arranged in columns and rows. Vertical clocks such as **802A**, **803A**, **802B** and **803B** cause the accumulated electrons in the image to transfer from one pixel to the next in the same column and

eventually to horizontal register **804A** or horizontal register **804B**. Horizontal clocks **805A**, **806A**, **805B**, **806B**, **805C**, **806C**, **805D** and **806D** control the transfer of electrons within the horizontal registers to outputs **808A**, **808B**, **808C** and **808D** via **807A**, **807B**, **807C** and **807D** which each comprise a charge-to-voltage converter, a buffer and, optionally, an amplifier. Although the horizontal and vertical clocks are shown as two-phase clocks, this is merely for illustrative purposes and does not limit how the invention may be used. Two, three or four phase clocks may be used for the horizontal and vertical clocks. The horizontal and vertical clocks need not have the same number of phases. In some embodiments the horizontal register is only on one side of the pixel array (such as horizontal register **804A**. Although each horizontal register is shown as divided in two, with each half transferring in opposite directions, the horizontal register may be a single register or, in preferred embodiments, may be divided into multiple segments which may all transfer in the same direction as one another. Hence the number of outputs may be greater than, or less than, the four shown. In one embodiment, there may be one output for every two columns.

The layout of part of one column of sensor **800** and other aspects of this sensor are further illustrated in FIG. **10** and described below in the descriptions of FIGS. **9** and **10**.

FIG. **9** illustrates aspects of the design, fabrication and operation of a backside-illuminated avalanche sensor **900**. Such a sensor may be fabricated with CMOS or CCD technology, or a combination thereof. Bipolar transistors (not shown) may be used in some of the circuits in combination with MOS transistors.

The sensor is fabricated in an intrinsic or lightly p-type doped (doping concentration less than or about $2 \times 10^{13} \text{ cm}^{-3}$) epitaxial layer **901** with a thickness that is between about 20 μm and about 200 μm (depending on the avalanche gain required, as well as other considerations such as the mechanical strength of the membrane after thinning the sensor). An n-type layer **904** (with, for example, a doping concentration of about 10^{16} cm^{-3}) is formed just under the top (front-side) surface of the epitaxial layer. Layer **904**, when the sensor is properly biased forms a buried channel that is used to collect and transfer electrons. At either end of the n-type layer **904** is a p+ type layer **905** which has about 2 \times or higher doping concentration than the n-type layer. The p+ type layer **905** is grounded by electrical contacts such as **912**. Layer **905** may be grounded in multiple locations.

A dielectric layer **908** is grown on the front surface of the epitaxial layer. Dielectric layer may comprise a single dielectric material, such as silicon dioxide, or it may comprise multiple layers of dielectric materials such as a silicon nitride layer on top of a silicon dioxide layer, or a three-layer stack such as silicon dioxide on silicon nitride on silicon dioxide. Typically dielectric layer thicknesses are in the range of about 50 nm to about 200 nm. Dielectric layer **908** has openings etched into it as appropriate to allow electrical contact to the underlying silicon where needed.

Multiple gate electrodes such as **920**, **930**, **935**, **940** and **945** are deposited and patterned on top of dielectric layer **908**. The gate electrodes are typically made of polysilicon or aluminum, but other conductive materials including other metals and semi-metallic compounds (such as TiN) may be used. Electrical connections such as **921**, **922**, **931**, **936**, **941** and **946** may be made to the gate electrodes.

In preferred embodiments, the gate electrodes overlap one another, as shown, for example at **932** in order to minimize and control fringe electric fields near the edges of the electrodes. The gate electrodes are separated by a dielectric material (not shown).

Circuits for amplifying or processing the signals and controlling the sensor may be fabricated inside the light sensitive area or adjacent to the light sensitive area. Such a circuit is illustrated by the MOSFET transistor formed by source/drain implants **906** (the source and drain are shown as having the same implants, but in some implementations the source and drain may be implanted differently), channel implant **906**, gate dielectric **909** and gate electrode **910**. Electrical connections may be made to this transistor, such as those shown as **916**, **917** and **915**. Typically such circuits comprise many transistors. One transistor is shown in FIG. **9** to illustrate key aspects of the inventive sensor without making the figure too complicated. An important aspect of the image sensors described herein is that MOSFET transistors with a n-type channel are fabricated in a p+ doped well **905** in order to electrically isolate them from dark currents and photocurrents in the epitaxial material **901**, as well as to shield the transistor from the backside voltage **911** (which is described below). Note that the gate dielectric **909** may be substantially similar to dielectric layer **908** and may be formed at the same time, or dielectric layer **909** may be formed of different materials and/or different thicknesses than dielectric layer **908** as necessary to get the desired transistor characteristics. Although a single MOSFET transistor is illustrated in FIG. **9**, NMOS, PMOS and bipolar transistors may be used as appropriate and may be electrically isolated by appropriate implanted layers such as **905** when necessary.

The back-side (light-sensitive) surface of epitaxial layer **901** is where light **999** is incident. A layer of pure boron **902** is deposited on the backside of epitaxial layer **901**. In preferred embodiments, boron layer **902** is between about 3 nm and 6 nm thick. Boron layers much thinner than about 3 nm may have pinholes that allow the silicon underneath to oxidize. Under prolonged exposure to DUV or VUV light, charges and traps accumulate in silicon dioxide. These charges and traps degrade the performance of the sensor. Boron layers thicker than about 6 nm are typically not preferred because boron absorbs UV, DUV and VUV light, so the sensitivity of the sensor would be reduced by a thick boron layer. Methods of depositing a pure boron layer on silicon are described in the '166 US patent application cited above and in references cited in the '166 patent application.

A very highly doped p+ layer **903** is formed at the backside surface of the epitaxial layer by incidental or deliberate drive-in of the boron during the deposition of pure boron layer **902**. In some embodiments, after depositing boron **902** on the backside of the epitaxial layer **901**, the wafer is held at an elevated temperature (such as between about 800° C. and about 950° C.) for between about one and five minutes in order to drive in some boron. Controlling the temperature and time allows the boron profile to be tailored.

Adjacent to layer **903** near the backside surface of the epitaxial layer is an n-type doped layer **970**. In a preferred embodiment, the thickness of n-type doped layer **970** is about 2 μm (such as a thickness between about 1 μm and 5 μm) and the concentration of the n-type dopant is about $2 \times 10^{16} \text{ cm}^{-3}$ (such as a dopant concentration of between about $5 \times 10^{15} \text{ cm}^{-3}$ and about 10^{17} cm^{-3}). Adjacent to n-type doped layer **970** is a thin highly doped p-type layer **971**. In a preferred embodiment, the dopant concentration in thin highly doped p-type layer **971** is about $2 \times 10^{19} \text{ cm}^{-3}$ (such as a dopant concentration between about $5 \times 10^{18} \text{ cm}^{-3}$ and about $5 \times 10^{19} \text{ cm}^{-3}$), and the thickness of thin highly doped p-type layer **971** is about 25 nm (such as a thickness between about 10 nm and about 50 nm). Other combinations of dopant concentration and thickness are possible. The total number of active p dopants in thin highly doped p-type layer **971** should exceed

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the total number of active dopants in n-type doped layer 970, so that layer 970 is fully depleted. For example, if the dopant concentration in thin highly doped p-type layer 971 is much higher than $2 \times 10^{19} \text{ cm}^{-3}$, layer 971 may be thinner than 25 nm.

An electrical connection 911 is made to the boron layer so that the backside of the sensor may be biased to a negative voltage between about -10V and about -400V in order to make the sensor operate as an avalanche sensor.

In a preferred embodiment, one or more antireflection layers 980 is deposited on the boron layer in order to reduce the reflectivity of the sensor at wavelengths of interest and so improve the sensitivity of the sensor at those wavelengths.

When light 999 is absorbed in the silicon electron hole pairs are created. Hole moves to the backside surface where they recombine, whereas electrons are accelerated towards the n type layer 904 by the bias voltage applied to backside by contact 911. Because n-type doped layer 970 is fully depleted by thin highly doped p-type layer 971, most of the bias voltage appears across layer 970, resulting in a strong electric field within that layer. That strong electric field ensures that most electrons will gain enough energy to create additional electron hole pairs by collision as they travel through n-type doped layer 970. In one exemplary embodiment with an applied bias voltage of about 50V (such as a bias voltage between about 10V and about 100V), many electrons (such as between about 10 to about 50) may be generated per absorbed incident photon from light 999. When an electron gain of less than about 10 is required, a thinner n-type doped layer 970 (such as one about 1 μm thick) may suffice, and/or a lower bias voltage may be used. The amplification of the number of electrons allows the signal to be increased relative to the intrinsic noise of the sensor. CMOS technology, which may be unsuitable for high-speed image inspection because of its non-Poisson noise statistics can be made suitable for image inspection by avalanche amplification that reduces the non-Poisson component of the noise relative to the increased signal level. With high enough gain, such as a gain of about 20 to 30, single photons may be detectable above the noise level of a CMOS or CCD sensor.

Gate 920 may have two or more electrical connections such as those shown as 921 and 922. In such embodiments gate 920 comprises a resistive material such as intrinsic or lightly doped polysilicon so that a potential difference is created between the two or more electrical contacts. This potential difference is used to control where the collected electrons accumulate in n-type layer 904. Electrons will accumulate under a local maximum of the voltage in the gate 920. For example if contact 921 is at a voltage of -5V and contact 922 is at a voltage of -1V, electrons will accumulate under 922. By using multiple contacts on gate 920, non-monotonic voltage profiles may be created to accumulate electrons at a location that is under a location away from either end of 920. When a small pixel (such as less than about 10 μm is used), a single potential on gate 920 may be used to cause electrons to accumulate in n-type layer 904 under gate 920.

By raising the voltage on gate 930 applied by contact 931, electrons accumulated near that gate will move underneath that gate. A higher voltage (such as 10V to 15V) can be used to move the electrons faster when high-speed operation is required. When the pixel is small (such as smaller than about 10 μm) and the desired speed of operation is not too high, the voltage on gate 930 may suffice to empty the charge from the pixel fast enough without the assistance of a voltage gradient on electrode 920. In preferred embodiments, a voltage gradient on electrode 920 as described above ensures that the electrons transfer quickly under gate 930.

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A more positive voltage than that applied to gate 930 (such as a few Volts more positive) is applied to gate 935 by contact 936. This causes the electrons to move rapidly under gate 936. The electrons can move in a few tens of nanoseconds. Lowering gate 930 to a voltage less than that applied by electrode 922 to gate 920 stops the transfer of electrons to the region under gate 935 and allows accumulation of the next image pixel under gate 920.

In one embodiment, such as sensor 700 illustrated in FIG. 7, a horizontal readout register comprises a series of gates similar to 940 arranged in a line perpendicular to the plane of FIG. 9. The electrons can be transferred from one gate to another by sequencing the voltages applied to the gates appropriately as is commonly used in CCDs. More, or fewer, gates may be used as required by the application. At the end of the horizontal register is a floating diffusion such as that shown under contact 948 for charge-to-voltage conversion. In sensor 700, the floating diffusion may not be located immediately adjacent to the light collecting pixel. It is so depicted in FIG. 9 merely for convenience. The operation of the floating diffusion is described below.

In another embodiment, such as sensor 600 illustrated in FIG. 6, there may be no horizontal readout register (and gate 940 may be omitted) and the electrons may be transferred directly to a floating diffusion such as the area under contact 948. A reset transistor such as that controlled by gate electrode 945 and connected to reset voltage 949 may be used to reset the floating diffusion prior to transferring the electrons from the pixel. The floating diffusion converts the charge of the electrons to a voltage and is routinely used in CCD sensors and CMOS sensors and will not be described in more detail here. Since the floating diffusion and reset transistor are in the light sensitive area in this embodiment, if necessary, the reset transistor and floating diffusion may be isolated from photocurrent and dark current by extending the p+ doped region 905 underneath the reset transistor and floating diffusion (as shown at 950). The output voltage on 948 may be connected to a buffer or amplifier before being connected to a row or column select, device output or analog to digital converter.

In sensor 600, each light sensitive pixel may have its own floating diffusion. In sensor 700, multiple pixels may share a floating diffusion through a horizontal register. In either case, the principles of operation of the floating diffusion are substantially similar.

There is more than one sequence in which the sensor of FIG. 9 may be fabricated. In one preferred embodiment, the front side doped regions (such as 904, 905, 906 and 907), the dielectric layers (such as 908 and 909) and polysilicon gate electrodes (such as 920 and typically some of the other gate electrodes) are formed while epitaxial layer 901 is on the surface of a wafer. In preferred embodiments, metal layers are not formed at this stage in the process. Then all, or part, of the wafer is removed by polishing and/or etching to expose, at least, the backside surface of the epitaxial layer in the light sensitive region of the sensor. Since the surface of the epitaxial layer adjacent to the wafer has a higher defect concentration than the bulk of the epitaxial layer, it is advantageous to polish or etch away a few microns of the backside of the epitaxial layer in order to improve the efficiency of the sensor.

Once the light sensitive area of the backside of the epitaxial layer is exposed, thin highly doped p-type layer 971 may be grown on that exposed surface by growing an epitaxial silicon layer with in-situ p-type doping at a very high dopant concentration. Then n-type doped layer 970 may be grown on layer 971 with in-site n-type doping. Since some boron (p-type dopant) may diffuse while layer 970 is being grown, layer 971 may be grown a little thinner and with higher dopant

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concentration than the final desired thickness and dopant concentration. Boron layer **902** can be deposited on n-type doped layer **970** and any additional needed drive-in of the boron to create layer **903** can be done. If desired, anti-reflection layer(s) may be deposited at this stage in the process, or later.

After the high temperature backside processes have been completed, metal layers may be deposited and patterned on the front surface.

In an alternative embodiment, n-type doped layer **970** is first grown epitaxially on a substrate wafer with in-situ n-type doping, then thin highly doped p-type layer **971** is grown epitaxially on top of n-type doped layer **970**. Then epitaxial layer **901** is grown epitaxially on top of highly doped p-type layer **971**. The entire front-side processing including metal layers may then be completed on the top surface of epitaxial layer **901** before exposing the backside of n-type doped layer **970**. Since it is important to minimize diffusion of the p-type dopant in high doped p-type layer **971** during subsequent processing steps, thermal processing should preferably be done using rapid thermal annealing rather than furnace processes. Pure boron layer **902** is then deposited on n-type doped layer **970**. A boron deposition temperature of about 450° C. may be used in order not to damage metal patterns on the front side. A laser or spike annealing process may be used to make the boron more uniform and to drive in some boron to form doped layer **903**.

Methods of fabricating a backside illuminated boron-coated image sensor are described in the '166 US patent application cited above. If the process of exposing the backside of the epitaxial layer does not remove all of the wafer, then that wafer must be intrinsic or very lightly doped (such as a doping concentration of less than about $2 \times 10^{13} \text{ cm}^{-3}$) or must be protected on its backside by a thick dielectric layer, in order that the wafer does not conduct under the reverse bias voltage applied to the backside of the epitaxial layer.

FIG. 10 illustrates aspects of the design, fabrication and operation of a backside-illuminated avalanche image sensor **1000** using CCD technology. Many features shown in FIG. 10 have substantially similar functions and are fabricated and operated in a substantially similar manner to the corresponding features of FIG. 9. Such features are labeled with the same label numbers as FIG. 9 and will not be described further here unless necessary to explain aspects specific to backside-illuminated avalanche image sensor **1000**.

In image sensor **1000**, a column of light sensitive pixels is formed under gates **1020**, **1022**, **1024** and **1026**. Electrical connections **1021**, **1023**, **1025** and **1027** are respectively made to these gates. Although only four gates are shown to avoid making the figure too cluttered, in preferred embodiments many more gates would be used in order to form a large number of light collecting pixels (such as between about 4 and 4000 pixels). The gates are used to control the storage of charge and to transfer stored charge from one pixel to another. As is well known in CCD technology, the gates may be configured as a two phase, three phase or four phase clock (i.e. there are two, three or four gates per pixel respectively). A two-phase clock can only transfer charge in one direction, and has the advantage of simplifying the driving electronics if transfer is only required in one direction. Three and four phase clocks have the advantage of being able to transfer stored charges in either direction. As is well known, one of the gates in each pixel must be held a few volts more positive (such as about 5V to 15V more positive) than ground while the adjacent electrodes are held a few volts negative relative to ground (such as about -5V to -15V) to attract electrons from the epitaxial layer **901** to near (but not at) the surface of the n+

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doped layer **904**, where they will be stored until the gate voltages are changed to cause that stored charge to be transferred. In a TDI sensor the gates will be clocked at a rate that causes the charge to be transferred in synchrony with a moving image falling on the sensor (such as in synchrony the motion of the stage on which the specimen being inspected is held).

Typically multiple columns of pixels are laid out in a 2D array similar to that illustrated in FIG. 8. Vertical clocks connected across the whole array are used to transfer one pixel to the next within all, or a group of, columns simultaneously. One or more horizontal registers are used to transfer the signals from each column to one or more outputs.

Any of the above described backside-illuminated avalanche image sensors may use sine wave clocks or arbitrary waveform clocks to control the transfer of charge in horizontal and/or vertical directions as appropriate. The generation and use of such clock waveforms is described in more detail in U.S. Pat. No. 7,609,309 entitled "Continuous Clocking of TDI Sensors" to Brown et al., U.S. Pat. No. 7,952,633 entitled "Apparatus for Continuous Clocking of TDI Sensors" to Brown et al., and U.S. Utility patent application Ser. No. 14/273,424 entitled "LOW-NOISE SENSOR AND AN INSPECTION SYSTEM USING A LOW-NOISE SENSOR" and filed on May 8, 2014 by Brown et al. All of these patents and applications are incorporated by reference herein.

Further details of anti-reflection coatings that may be applied to the boron coating on the backside of the sensor can be found in U.S. patent application Ser. No. 12/476,190 entitled "Anti-Reflective Coating For Sensors Suitable For High Throughput Inspection Systems" and filed on Jun. 1, 2009 by Brown, and in U.S. patent application Ser. No. 14/591,325 entitled "Anti-reflection Layer for Back-Illuminated Sensor" and filed by Muramatsu et al. on Jan. 7, 2015. Both of these applications are incorporated by reference herein.

The various embodiments of the structures and methods of this invention that are described above are illustrative only of the principles of this invention and are not intended to limit the scope of the invention to the particular embodiments described. For example, the pixels of the sensors could be laid out in different configurations than those shown, and may comprise more or fewer pixels than shown, or the number of outputs could be larger or smaller than shown. In some embodiments only one or two outputs may be used. In preferred embodiments that are suited to use in high-speed inspection systems such as those used in the semiconductor industry (some of which are described herein), multiple outputs (such as several tens of outputs, a few hundred outputs, or one output per every two columns) are used to simultaneously output multiple pixels in order to achieve a high data output rate. Such sensors may comprise a linear array of about 1000 or a few thousand pixels, or may comprise a 2D array of about 1000 or a few thousand columns and between a few hundred and a few thousand pixels long.

The invention claimed is:

1. A backside-illuminated avalanche sensor comprising: an epitaxial silicon layer; a thin highly doped p-type layer, an n-type doped layer and a boron layer disposed on a light-sensitive surface of the epitaxial silicon layer; and circuits formed on an opposing surface of the epitaxial silicon layer, wherein the epitaxial silicon layer comprises one of intrinsic silicon and p-type doped silicon with less than 2×10^{13} dopant atoms per cubic centimeter (cm^{-3}), wherein the circuits comprise an n-type doped buried channel,

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wherein at least some of the circuits are fabricated in a grounded p+ well with a dopant concentration greater than 10^{16} dopant atoms cm^{-3} ,
 wherein the thin highly doped p-type layer comprises p-type doped silicon with a dopant concentration greater than 5×10^{18} dopant atoms cm^{-3} , and a thickness of less than 50 nm, and
 wherein the n-type doped layer comprises n-type doped silicon with a dopant concentration between 5×10^{15} dopant atoms cm^{-3} and 10^{17} dopant atoms cm^{-3} , and a thickness of between 1 μm and 5 μm .
 2. The sensor of claim 1,
 wherein the boron layer comprises pure boron having a thickness in the range of 2 nm to 6 nm, and
 wherein the sensor further comprises one or more anti-reflection layers disposed on the boron layer.
 3. The sensor of claim 1, wherein the sensor further comprises means for maintaining the boron layer at a negative potential of between -10V and -400V relative to the opposing surface of the epitaxial layer.
 4. The sensor of claim 1, wherein the circuits comprise at least one of CMOS image circuits, CCD circuits and bipolar transistors.
 5. The sensor of claim 1, wherein the sensor comprises a linear array sensor.
 6. The sensor of claim 1, wherein the sensor comprises a two-dimensional array of pixels.
 7. The sensor of claim 6, wherein each pixel comprises circuits including a floating diffusion region configured for charge-to-voltage conversion.
 8. A system for inspecting a sample, the system comprising:
 an illumination source comprising a UV laser for illuminating the sample;
 image relay optics configured to direct light outputs, reflections, or transmissions, of the sample to a first channel image mode relay when the light outputs correspond to the first channel, and to a second channel image mode relay when the light outputs correspond to the second channel; and
 a sensor configured to receive relay outputs of the first channel image mode relay and the second channel image mode relay,
 wherein the sensor comprises an epitaxial silicon layer comprising one of intrinsic and p-type doped silicon having a doping concentration of less than 2×10^{13} dopant atoms cm^{-3} , a pure boron coating on a light-sensitive surface of the epitaxial layer, and circuits formed on an opposite surface of the epitaxial layer, the circuits comprising an n-type doped buried channel, and further wherein at least some of the circuits are fabricated in a grounded p+ well with a dopant concentration greater than 10^{16} dopant atoms cm^{-3} , and
 wherein the system further includes a voltage source configured to maintain the boron surface at a negative potential of between -10V and -400V relative to the opposite surface.
 9. The system of claim 8, wherein the sensor further comprises an anti-reflection coating is applied to the surface of the pure boron coating.
 10. The system of claim 8, wherein the sensor further comprises an n-type doped layer adjacent to the pure boron coating, said n-type doped layer having a thickness between 1 μm and 5 μm and comprising n-type doped silicon with a dopant concentration between 5×10^{15} dopant atoms cm^{-3} and 10^{17} dopant atoms cm^{-3} .

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11. The system of claim 8, wherein the circuits are fabricated using at least one of CMOS, CCD or bipolar technology.
 12. A surface inspection apparatus comprising:
 an illumination system configured to generate a focused beam of UV, DUV or VUV laser radiation at a non-normal incidence angle relative to a surface to form an illumination line on the surface substantially in a plane of incidence of the focused beam, wherein the plane of incidence is defined by the focused beam and a direction that is through the focused beam and normal to the surface;
 a collection system configured to image the illumination line, wherein the collection system comprises:
 an imaging lens for collecting light scattered from a region of the surface comprising the illumination line;
 a focusing lens for focusing the collected light; and
 a sensor comprising an array of light sensitive elements, wherein each light sensitive element of the array of light sensitive elements is configured to detect a corresponding portion of a magnified image of the illumination line,
 wherein the sensor comprises an epitaxial silicon layer comprising one of intrinsic and p-type doped silicon having a doping concentration of less than 2×10^{13} dopant atoms cm^{-3} , a pure boron coating on a light-sensitive surface of the epitaxial layer, and circuits formed on an opposite surface of the epitaxial layer, the circuits comprising an n-type doped buried channel, and further wherein at least some of the circuits are fabricated in a grounded p+ well with a dopant concentration greater than 10^{16} dopant atoms cm^{-3} , and
 wherein the illumination system further includes a voltage source configured to maintain the boron surface at a negative potential of between -10V and -400V relative to the opposite surface.
 13. A wafer inspection system comprising:
 a UV, DUV or VUV laser for generating an output beam;
 means for focusing the output beam on a wafer; and
 means for collecting scattered light from the wafer and directing the scattered light to an image sensor,
 wherein the image sensor comprises an epitaxial silicon layer comprising one of intrinsic and p-type doped silicon having a doping concentration of less than 2×10^{13} dopant atoms cm^{-3} , a pure boron coating on a light-sensitive surface of the epitaxial layer, and circuits formed on an opposite surface of the epitaxial layer, the circuits comprising an n-type doped buried channel, and further wherein at least some of the circuits are fabricated in a grounded p+ well with a dopant concentration greater than 10^{16} dopant atoms cm^{-3} , and
 wherein the wafer inspection system further includes a voltage source configured to maintain the boron surface at a negative potential of between -10V and -400V relative to the opposite surface.
 14. The wafer inspection system of claim 13, wherein the sensor further comprises an n-type doped layer adjacent to the pure boron coating, said n-type doped layer having a thickness between 1 μm and 5 μm and comprising n-type doped silicon with a dopant concentration between 5×10^{15} dopant atoms cm^{-3} and 10^{17} dopant atoms cm^{-3} .

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15. An optical system for detecting anomalies of a sample, the optical system comprising:

- a laser for generating an output beam;
- first optics directing the first beam along a first path onto a first spot on a surface of the sample;
- second optics directing the second beam along a second path onto a second spot on the surface of the sample, the first and second paths being at different angles of incidence to the surface of the sample;
- a first detector;
- collection optics including a curved mirrored surface for receiving scattered radiation from the first spot or the second spot on the sample surface and focusing the scattered radiation to the first detector, the first detector providing an output value in response to the radiation focused onto it by the curved mirrored surface; and
- an instrument causing relative motion between the first and second beams and the sample so that the first and second spots are scanned across the surface of the sample,

wherein the detector includes an sensor, the sensor comprising an epitaxial silicon layer which is intrinsic or p-type doped with less than 2×10^{13} dopant atoms cm^{-3} , a pure boron coating on the light-sensitive surface of the epitaxial layer, and circuits formed on the opposite surface of the epitaxial layer, the circuits comprising an n-type doped buried channel, and further wherein at least some of the circuits are fabricated in a grounded p+ well with a dopant concentration greater than 10^{16} dopant atoms cm^{-3} , and the boron surface is held at a negative potential of between 10V and 400V relative to the opposite surface.

16. A catadioptric imaging system comprising:

- a UV, DUV or VUV light source;
- adaptation optics for controlling an illumination beam size and profile on a surface being inspected;
- an objective including a catadioptric objective, a focusing lens group, and a zooming tube lens section in operative relation to each other; and
- a prism for directing the UV light along the optical axis at normal incidence to a surface of a sample and directing specular reflections from surface features of the sample as well as reflections from optical surfaces of the objective along an optical path to an image sensor located at an imaging plane,

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wherein the image sensor comprises an epitaxial silicon layer which is intrinsic or p-type doped with less than 2×10^{13} dopant atoms cm^{-3} , a pure boron coating on the light-sensitive surface of the epitaxial layer, and circuits formed on the opposite surface of the epitaxial layer, the circuits comprising an n-type doped buried channel, and further wherein at least some of the circuits are fabricated in a grounded p+ well with a dopant concentration greater than 10^{16} dopant atoms cm^{-3} , and the boron surface is held at a negative potential of between 10V and 400V relative to the opposite surface.

17. The catadioptric imaging system of claim 16, wherein the sensor further comprises an n-type doped layer adjacent to the pure boron coating, said n-type doped layer having a thickness between about 1 μm and about 5 μm and comprising n-type doped silicon with a dopant concentration between 5×10^{15} dopant atoms cm^{-3} and 10^{17} dopant atoms cm^{-3} .

18. A method of fabricating a backside-illuminated avalanche image sensor, the method comprising:

- forming an intrinsic or p-doped silicon epitaxial layer on a silicon wafer with a p-dopant concentration less than 2×10^{13} atoms cm^{-3} ;

- forming at one of CMOS, CCD and bipolar circuits on a front-side surface of the epitaxial layer, said circuits comprising at least a buried n-type channel, and at least part of those circuits are formed in a p+-doped well with a doping concentration greater than 10^{16} atoms cm^{-3} ;

- polishing or etching away the silicon wafer to expose a back-side surface of the epitaxial layer in at least a light sensitive area;

- epitaxially growing a p-type layer on the exposed surface with a dopant concentration greater than 5×10^{18} dopant atoms cm^{-3} ;

- epitaxially growing an n-type layer on the exposed surface with a dopant concentration between 5×10^{15} dopant atoms cm^{-3} and 10^{17} dopant atoms cm^{-3} ; and

- depositing a pure boron coating on the exposed back-side surface of the epitaxial layer such that the boron coating is coupled to a negative potential of between -10V and -400V relative to the front-side surface of the epitaxial layer.

19. The method of claim 18, further comprising depositing an anti-reflection coating on the pure boron coating.

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